PRO-LOG®
CORPORATION

# STD 7000

# 78C13 CMOS Z80 Processor Card

# USER'S MANUAL

5/84

# FOREWORD

This manual explains how to use Pro-Log's 78C13 CMOS Z80 CPU card. It is structured to reflect the answers to basic questions that you, the user, might ask yourself about the 78C13. We welcome your suggestions on how we can improve our instructions.

The 78C13 is part of Pro-Log's Series 7000 STD BUS hardware. Our products are modular, and they are designed and built with second-sourced parts that are industry standards. They provide the industrial manager with the means of using his own people to control the design, production, and maintenance of the company's products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, to provide maximum assistance to the user, we teach courses on how to design with, and to use, microprocessors and STD BUS products.

You may find the following Pro-Log documents useful in your work: the **Microprocessor User's Guide** and the **Series 7000 STD BUS Technical Manual**. If you would like a copy of these publications, please submit your request on your company letterhead.

# Contents


| | Page |
|---|---|
| **Foreword** | ii |
| **Figures** | iv |
| **References and Bibliography** | v |
| **Section 1 - Purpose and Main Features** | 1-1 |
| Purpose | 1-1 |
| Features | 1-1 |
| Functional Description | 1-3 |
| **Section 2 - Installation and Specifications** | 2-1 |
| Introduction | 2-1 |
| Installation | 2-1 |
| CMOS Precautions | 2-2 |
| Termination and Loading | 2-2 |
| Jumpers | 2-2 |
| Cabling | 2-2 |
| Memory Devices (W3,W4,W11-W14,W15-W18) | 2-4 |
| MEMEX and Segment (W2,W5,W7,W10) | 2-5 |
| Onboard Port (W6,W8) | 2-6 |
| IOEXP (W1) | 2-6 |
| Timing Specifications | 2-6 |
| Mechanical Specifications | 2-6 |
| Electrical and Environmental Specifications | 2-16 |
| **Section 3 - Operation and Programming** | 3-1 |
| Introduction | 3-1 |
| Power-On and Pushbutton Reset Circuit | 3-1 |
| MEMEX and Segment Control | 3-2 |
| **Section 4 - Operating Software** | 4-1 |
| **Section 5 - Maintenance** | 5-1 |
| Reference Drawings | 5-1 |
| Return for Repair Procedures | 5-5 |
| Limited Warranty | 5-5 |

# Figures


| Figure | | Page |
|---|---|---|
| 1-1 | 78C13 CMOS Z80 Processor Card | 1-1 |
| 1-2 | 78C13 Functional Block Diagram | 1-2 |
| 2-1 | Installation | 2-1 |
| 2-2 | Jumper Functions | 2-2 |
| 2-3 | Physical Layout of Jumpers | 2-3 |
| 2-4 | 24-Pin Device in a 28-Pin Socket | 2-4 |
| 2-5 | 2K x 8 Configuration Options | 2-4 |
| 2-6 | 2K x 8 Decoder Configurations | 2-4 |
| 2-7 | 8K x 8 Configuration Options | 2-4 |
| 2-8 | 8K x 8 Decoder Configurations | 2-5 |
| 2-9 | Recommended Memory Components | 2-5 |
| 2-10 | MEMEX Affecting Onboard Memory | 2-5 |
| 2-11 | MEMEX Port Configuration | 2-5 |
| 2-12 | Segment Port Configuration | 2-5 |
| 2-13 | Onboard Port Configuration | 2-6 |
| 2-14 | Opcode Fetch and Refresh Timing | 2-7 |
| 2-15 | Memory Read Timing Other than Opcode Fetch | 2-8 |
| 2-16 | Memory Write Timing | 2-9 |
| 2-17 | Output Timing | 2-10 |
| 2-18 | Input Timing | 2-11 |
| 2-19 | Bus Request Timing | 2-12 |
| 2-20 | Interrupt Request Timing | 2-13 |
| 2-21 | Nonmaskable Interrupt Request Timing | 2-14 |
| 2-22 | Wait State Timing | 2-15 |
| 2-23 | Electrical and Environmental Specifications | 2-16 |
| 2-24 | Segment Connector Pin List | 2-16 |
| 2-25 | STD Edge Connector | 2-16 |
| 3-1 | Example of MEMEX for Selecting Between Two Banks of Memory in a 96K Memory System | 3-3 |
| 3-2 | Example of MEMEX for Selecting Between Two Banks of Memory in a 128K Memory System | 3-3 |
| 5-1 | Schematic (Page 1) | 5-2 |
| 5-2 | Schematic (Page 2) | 5-3 |
| 5-3 | Assembly Drawing | 5-4 |

# REFERENCES/BIBLIOGRAPHY

**Series 7000 STD BUS Technical Manual**, Monterey CA: Pro-Log Corporation.

**HS-C²MOS Integrated Circuits Technical Data**, 2nd edition, Tokyo, Japan: Toshiba Corporation, 1983 K 4107.

**1982/83 Data Book**, 1st edition, Campbell, CA: Zilog Corporation, 1982, 00-2034-02: pps 5-27.

**Technical Literature for CMOS Z80 CPU Model no. LH5080/LH5080L**, Paramus, NJ: Sharp Electronics Corporation, November 1982, Doc. No. KS-82454.

# SECTION 1
# Purpose and Main Features

## PURPOSE

The 78C13 combines the advantages of CMOS logic and a CMOS CPU with onboard memory and memory expansion controls.

The memory consists of four JEDEC standard 28-pin sockets, which can be configured for 8K x 8 or 2K x 8 static CMOS RAM, PROM, or EPROM. Address, data, and control buses are bidirectional which allows external access to on-card memory.

Onboard I/O ports control MEMEX and Segment, so that the 78C13 can control expanded memory schemes.

Fully implemented in high speed CMOS, the 78C13 offers high noise immunity, low power consumption, and a wide temperature range. It is designed to be used with other CMOS cards on the STD BUS.

## FEATURES

- Fully CMOS: high noise immunity, low power consumption, wide temperature range
- CMOS Z80 processor
- 32K byte capacity with four 8K x 8 memory devices or 8K byte capacity with four 2K x 8 memory devices
- DMA to onboard memory sockets
- 2.5 MHz crystal
- Dynamic RAM refresh control
- Power-on reset with Vcc sensing
- MEMEX and Segment memory expansion control
- Single +5V operation

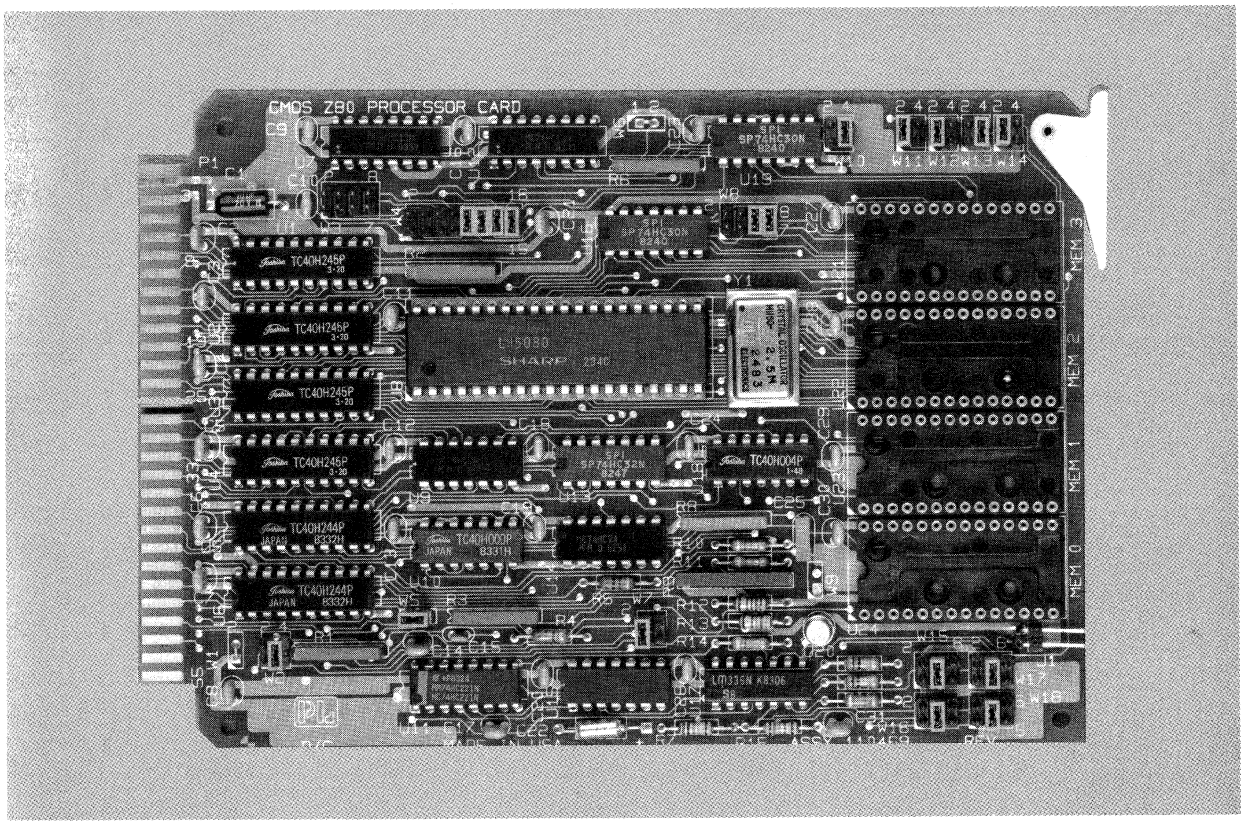



Figure 1-1. 78C13 CMOS Z80 Processor Card

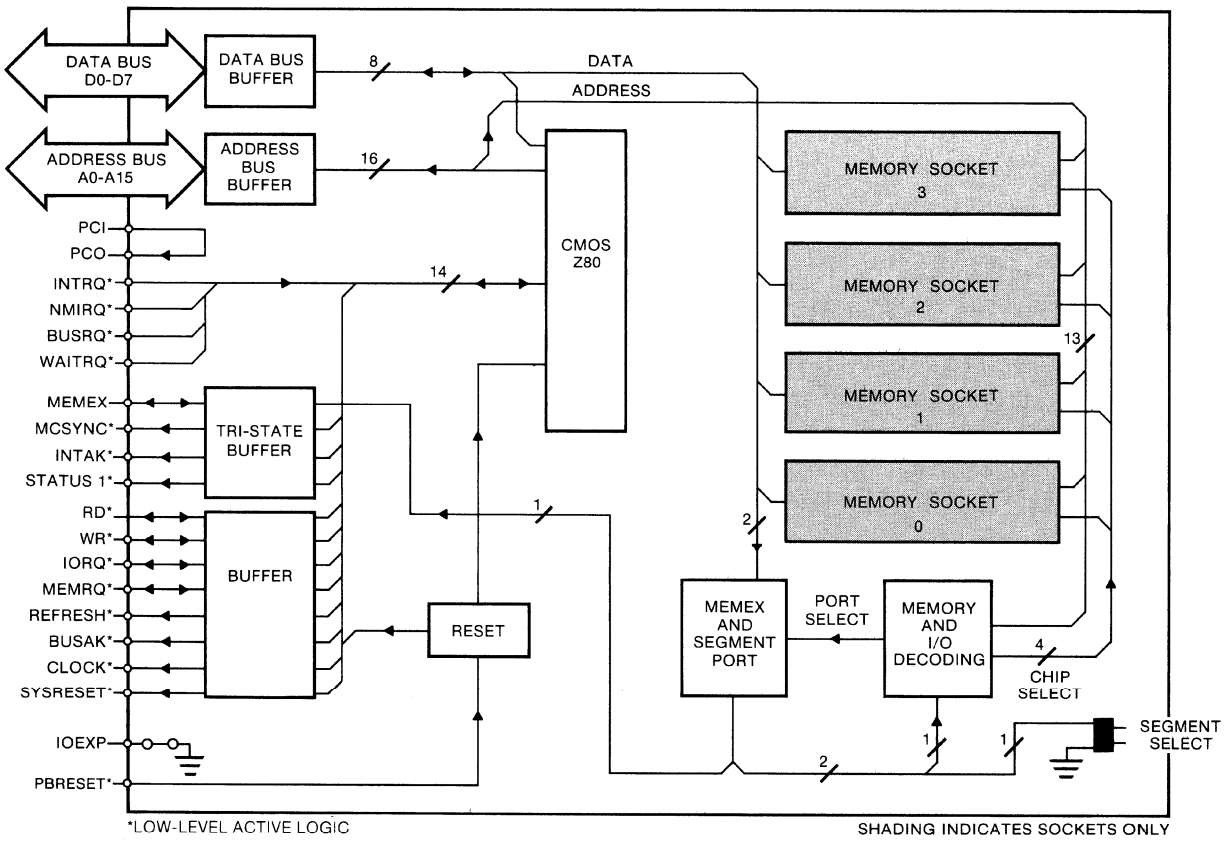



Figure 1-2. 78C13 Functional Block Diagram

## FUNCTIONAL DESCRIPTION

This portion of section 1 describes the function of each block of circuitry shown in the Functional Block Diagram of figure 1-2.

### CMOS Z80 CPU

The CMOS Z80 CPU is a CMOS version of the industry standard Z80. All the functions, features, and capabilities of a Z80 are coupled with the advantages of CMOS technology; high noise immunity, low power consumption, and wide temperature range. The result is a CPU with proven features that can use existing software and that can be used under extreme conditions. Note that the part number for the CMOS Z80 may not include "Z80."

### Onboard Memory

The onboard memory capability consists of four 28-pin sockets. This memory can be 32K bytes consisting of a combination of four 8K x 8 RAMs or ROMs, or it can be 8K bytes consisting of a combination of four 2K x 8 RAMs or ROMs. The 2K parts cannot be mixed with the 8K parts.

### Memory Decode

The memory decode consists of both an 8K x 8 and a 2K x 8 memory decoder. This circuitry decodes the memory address lines into 8K and 2K blocks to select the addressed memory socket. For more information, see section 2, **Installation and Specifications.**

### I/O Decode

The I/O decode section selects the onboard port and decodes the address lines only during an I/O write cycle. MEMEX and Segment can be written through the onboard port.

### Reset

The reset circuit resets the CPU during power-up or during a pushbutton reset. During power-up, the circuit keeps the CPU in a reset state until the power supply reaches a voltage in the proper operating range. This delay ensures that the CPU has a valid power supply when it leaves reset, which prevents latch-up. The pushbutton reset circuit debounces the pushbutton input and then shortens the pulse width and synchronizes it with the M1* signal to avoid interference with refresh of any dynamic RAM.

### MEMEX and Segment Port

Both the STD BUS memory expansion line, MEMEX, and the user card edge memory expansion line, Segment, are controlled by the on-card port of the 78C13. Both signals provide control to expand memory for large systems. See section 3, **Operation and Programming**, for more detail.

## CMOS PRECAUTIONS

1. An input to a CMOS gate should not exceed its power supply range. If a high level input exceeds the power supply voltage, current will flow into the input through the input protection diode. This may result in latch-up or damage.
2. Because of this restriction, in systems using two power supplies special attention should be paid to the relative voltage levels of the two supplies when each supply is turned on, and the difference in rise and fall times between the two supplies. One way to avoid possible problems when using two supplies is to connect them to each other, directly or through diodes.
3. To prevent damage to CMOS components by static discharge, the card should always be stored in a conductive carrier. Individuals and tools should be grounded before coming in contact with the card.

## TERMINATION AND LOADING

A termination network is not required for Pro-Log's CMOS STD BUS systems. (In fact, using Pro-Log's 7909A terminator card in a CMOS STD system will degrade the system performance as a result of its capacitive loading.)

Since the input impedance of CMOS is very large, the main restriction on fanout is load capacitance. As the total capacitive load on an output is increased, the propagation delays increase, along with power consumption. Since Pro-Log's 24- slot 7106 motherboard uses termination that presents a large capacitive load, it should not be used with CMOS cards. The user should check any other termination in the system for capacitive and DC loading.

## JUMPERS

There are several optional functions on the 78C13 which are selected by jumpers. Most of the jumpers are wirewrap posts which can be shorted by supplied shorting plugs (Elco Corporation, part number 00 8261 02 42 00 870), or by wirewrapping. Two of the card jumpers are soldered wire. To disconnect them, cut each wire jumper in two places to prevent reshorting. The wire jumpers can be replaced with a pair of wirewrap posts (Elco Corporation, part number 00 8261 02 32 00 852). When removing wire jumpers, be sure to cut them and remove one half at a time to prevent circuit trace damage.

## CABLING

The J1 Segment connector can use a Pro-Log RC704-1 or RC704-2 cable. These cables have a 2-pin connector on each end, with one (RC704-1) or two (RC704-2) feet of twisted pair wire. These cables mate to the card responding to Segment (e.g., Pro-Log's 77C02 CMOS 16K memory card).

| JUMPER | | DESCRIPTION | As Shipped |
|---|---|---|---|
| W1 | 1-2 | IOEXP is connected to ground. | 1-2 |
| | no jumper | IOEXP must be controlled by another card. | |
| W2 | 1-2 | Segment is low at power-up and its port is noninverting. | 3-4 |
| | 3-4 | Segment is high at power-up and its port is inverting. | |
| W3 | | Selects memory address ranges for 2K x 8 memory devices, see figure 2-6. | no jumper |
| W4 | | Selects memory address ranges for 8K x 8 memory devices, see figure 2-8. | 9-10, 11-12, 13-14, 15-16 |
| W5 | 1-2 | The 78C13 controls MEMEX. | 1-2 |
| | no jumper | MEMEX must be controlled by another card. | |
| W6 | 1-2 | MEMEX and Segment port enabled. | 1-2 |
| | no jumper | MEMEX and Segment port disabled. | |
| W7 | 1-2 | MEMEX is low at power-up, and its port is noninverting. | 1-2 |
| | 3-4 | MEMEX is high at power-up, and its port is inverting. | |
| W8 | 1-2, 3-4 | MEMEX and Segment control port address is 7F. | 5-6, 7-8 |
| | 5-6, 7-8 | MEMEX and Segment control port address is FE. | |
| W9 | no jumper | Reserved for Pro-Log use | no jumper |
| W10 | 1-2 | On-card memory responds to MEMEX high if enabled. | 3-4 |
| | 3-4 | On-card memory responds to MEMEX low if enabled. | |
| | no jumper | On-card memory is independent of MEMEX. | |
| W11 | W11-W14 | Select RAM or ROM for MEM 3 to MEM 0 | 1-2 |
| W12 | | respectively for 8K x 8 devices. | 1-2 |
| W13 | | | 1-2 |
| W14 | 1-2 | The memory socket is RAM. | 3-4 |
| | 3-4 | The memory socket is ROM. | |
| W15 | W15-W18 | Configure MEM 0 to MEM 3 respectively | 3-4 |
| W16 | | for RAM/ROM, 2K/8K memory sockets. | 3-4 |
| W17 | | | 3-4 |
| W18 | 1-2 | The memory socket is 2K x 8 ROM. | 3-4 |
| | 3-4 | The memory socket is 8K x 8. | |
| | 5-6 | The memory socket is 2K x 8 RAM. | |

Figure 2-2. Jumper Functions (78C13)

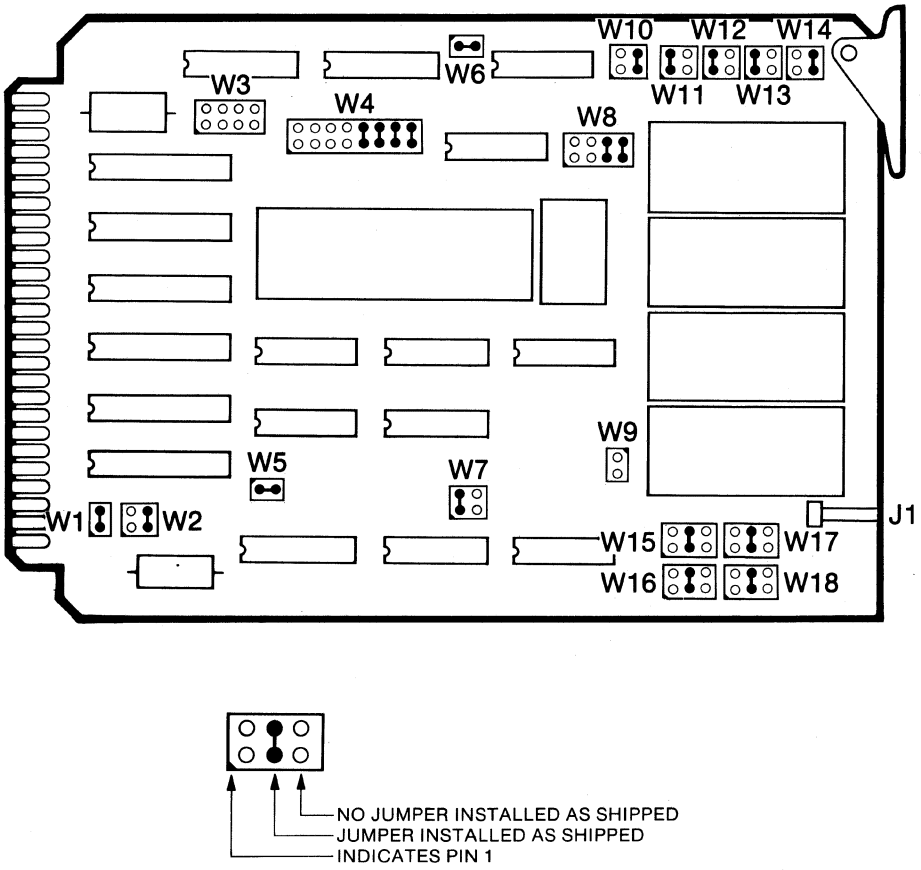



Figure 2-3. Physical Layout of Jumpers (78C13)

## MEMORY DEVICES (W3, W4, W11-W14, W15-W18)

The 78C13 has four 28-pin sockets that can be configured for a combination of 2K x 8 RAMs or ROMs or a combination of 8K x 8 RAMs or ROMs. The decoding scheme does not allow mixing the 2K devices with the 8K devices. The sockets are configured to JEDEC 28-pin standards. When using 24-pin 2K x 8 memory chips, place them in the bottom of the socket as shown in figure 2-4.

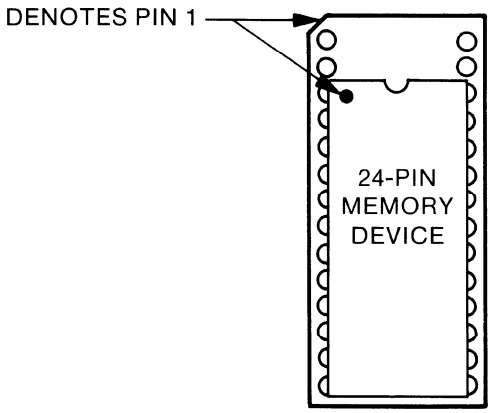



Figure 2-4. 24-Pin Device in a 28-Pin Socket

When using 2K x 8 devices, configure W15 through W18 as shown in figure 2-5.

| PART | W15-W18 JUMPER PIN NUMBERS |
|---|---|
| 2K ROM/PROM/EPROM | 1-2 |
| 2K RAM | 5-6 |

Figure 2-5. 2K x 8 Configuration Options

The decoding scheme for W3, the 2K x 8 decoder jumper, is shown in figure 2-6.

| W3 PIN NO. | SOCKET AFFECTED | ADDRESS RANGE |
|---|---|---|
| 7-8 | MEM 0 | 0000-07FF |
| 5-6 | MEM 1 | 0800-0FFF |
| 3-4 | MEM 2 | 1000-17FF |
| 1-2 | MEM 3 | 1800-1FFF |

Figure 2-6. 2K x 8 Decoder Configurations

To disable any of the onboard memory sockets, remove the associated jumpers from W3 for the specific address range. When using 2K x 8 devices **DO NOT** have jumpers in W4, or false addressing will result.

When using 8K x 8 devices, jumpers W15 through W18 are configured with pins 3-4 jumpered. Also jumpers W11 through W14 are configured as shown in figure 2-7.

| PART | W11-W14 JUMPER PIN NUMBERS |
|---|---|
| 8K RAM | 1-2 |
| 8K ROM/PROM/EPROM | 3-4 |

Figure 2-7. 8K x 8 Configuration Options

The decoding scheme for 8K x 8 devices involves jumper W4. Figure 2-8 shows the address location for each jumper.

| W4 PIN NO.* | SOCKET AFFECTED | ADDRESS RANGE |
|---|---|---|
| 15-16 | MEM 0 | 0000-1FFF |
| 7-8 | | 8000-9FFF |
| 13-14 | MEM 1 | 2000-3FFF |
| 5-6 | | A000-BFFF |
| 11-12 | MEM 2 | 4000-5FFF |
| 3-4 | | C000-DFFF |
| 9-10 | MEM 3 | 6000-7FFF |
| 1-2 | | E000-FFFF |

* Only one jumper should be installed per memory socket.

Figure 2-8. 8K x 8 Decoder Configurations

To disable any of the onboard memory sockets, remove the associated jumpers from W4 for the specific address range. When using 8K x 8 devices **DO NOT** have jumpers in W3, or false addressing will result.

Figure 2-9 shows a list of memory devices which have been tested for the 78C13 card. To use other memory components, compare the manufacturers' data sheets to the socket configurations, check for any special requirements, and be sure they are designed to be used with CMOS logic.

| MEMORY TYPE | MANUFACTURER | PART NUMBER |
|---|---|---|
| 2K RAM | OKI | MSM5128 |
| 2K EPROM | National Semiconductor | NM27C16Q-55 |
| 8K RAM | Hitachi | HM6264-15 |
| 8K EPROM | Fujitsu | MBM27C64-25 |

Figure 2-9. Recommended Memory Components

## MEMEX AND SEGMENT (W2,W5,W7,W10)

MEMEX and Segment are both controls for expanded memory schemes. For more detailed information, see section 3, **Operation and Programming**.

Several jumpers affect MEMEX. W10 determines how MEMEX affects onboard memory. Figure 2-10 shows the positions of W10 with relationship to MEMEX.

| W10 JUMPER POSITION | ONBOARD MEMORY ENABLED |
|---|---|
| 1-2 | MEMEX high |
| 3-4* | MEMEX low |

* As shipped configuration.

Figure 2-10. MEMEX Affecting Onboard Memory

If no pins of W10 are jumpered, then the onboard memory is permanently enabled, regardless of the state of MEMEX.

Jumper W7 determines the state of MEMEX after reset and whether the data written to the MEMEX port is to be inverted. Figure 2-11 shows the possible configurations.

| W7 PIN NO. | STATE AFTER RESET | DATA FROM PORT |
|---|---|---|
| 1-2* | MEMEX low | Noninverted |
| 3-4 | MEMEX high | Inverted |

* As shipped configuration.

Figure 2-11. MEMEX Port Configuration

Jumper W5 determines which card controls MEMEX. With the jumper installed, MEMEX is controlled by the 78C13. Otherwise, MEMEX is left floating to be controlled by another card.

W2 determines the state of Segment after reset and whether the data written to the Segment port is to be inverted. Figure 2-12 shows the possible configurations.

| W2 PIN NO. | STATE AFTER RESET | DATA FROM PORT |
|---|---|---|
| 1-2 | Segment low | Noninverted |
| 3-4* | Segment high | Inverted |

* As shipped configuration.

Figure 2-12. Segment Port Configuration

## ONBOARD PORT (W6,W8)

Jumpers W6 and W8 affect the configuration of the onboard port through which data for MEMEX and Segment are passed. If W6 is installed, the port is enabled, if W6 is not installed, the port is disabled. Jumper W8 determines the address of the port. Figure 2-13 shows the possible configurations.

| W8 PIN NUMBERS | PORT ADDRESS |
|---|---|
| 5-6, 7-8* | Port FE |
| 1-2, 3-4 | Port 7F |

* As shipped configuration.

Figure 2-13. Onboard Port Configuration

## IOEXP (W1)

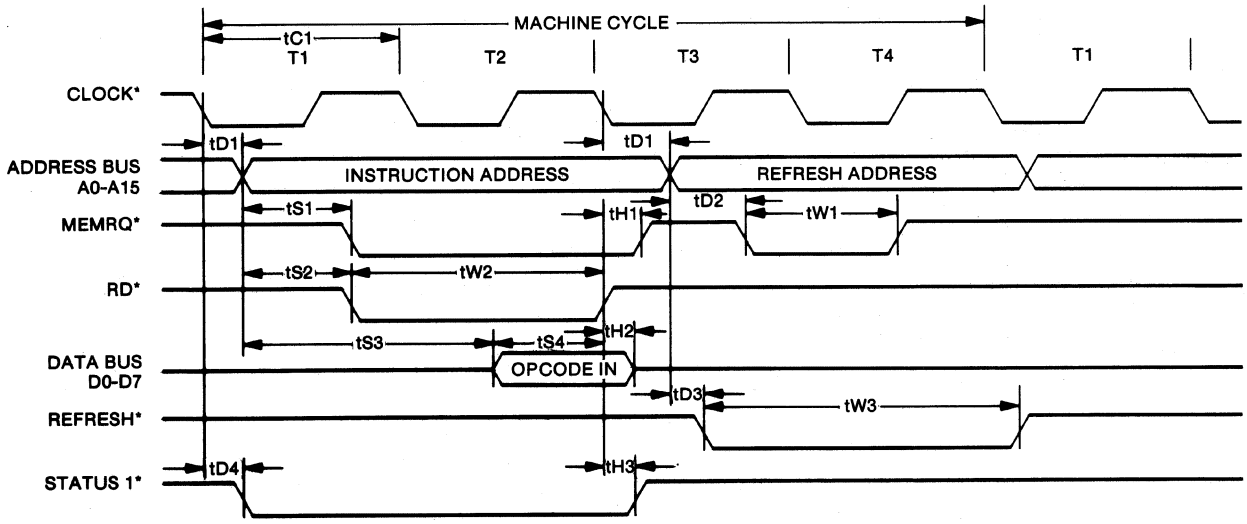
IOEXP is one of the STD BUS standard signals. IOEXP enables or expands I/O port addressing. Jumper W1 determines which card controls the IOEXP line. With the jumper installed, IOEXP is grounded by the 78C13. With no jumper, IOEXP is left floating to be controlled by another card.

## TIMING SPECIFICATIONS

Figures 2-14 through 2-22 give timing specifications for the 78C13 card.

## MECHANICAL SPECIFICATIONS

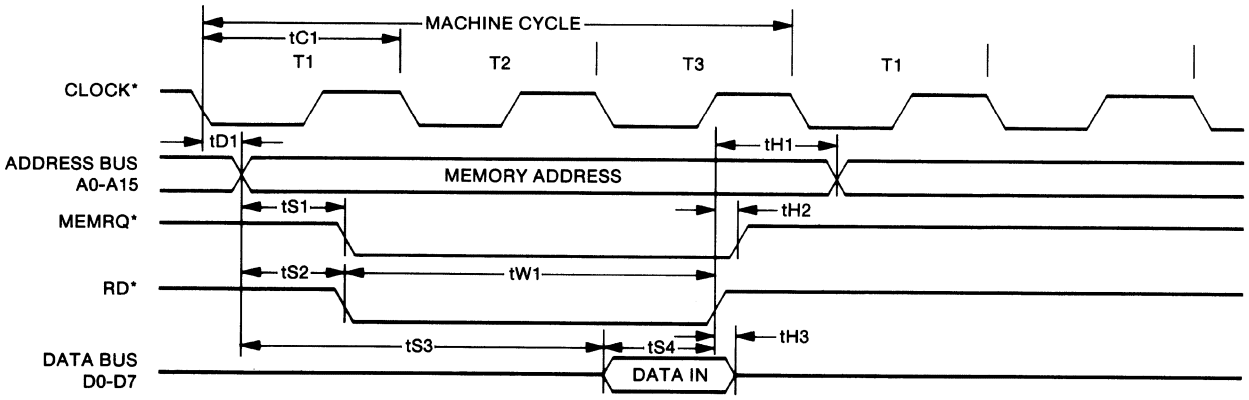
The 78C13 meets all general mechanical specifications of the STD BUS. Refer to the STD Specification and Practice for outline dimensions.




| SYMBOL | PARAMETER | MIN | MAX |
|---|---|---|---|
| tC1 | Clock cycle time | 400 | — |
| tD1 | Address delay from CLOCK* | — | 210 |
| tD2 | MEMRQ* delay from Refresh Address valid | — | 195 |
| tD3 | REFRESH* delay from Refresh Address valid | — | 100 |
| tD4 | STATUS 1* delay from CLOCK* | — | 195 |
| tH1 | MEMRQ* hold time after RD* inactive | 0 | — |
| tH2 | Data hold time after RD* inactive | 0 | — |
| tH3 | STATUS 1* hold time after RD* inactive | 0 | — |
| tS1 | Address setup before MEMRQ* active | 45 | — |
| tS2 | Address setup before RD* active | 105 | — |
| tS3 | Address setup before Data valid | 440 | — |
| tS4 | Data setup before RD* inactive | 300 | — |
| tW1 | MEMRQ* pulse width (REFRESH) | 300 | — |
| tW2 | RD* pulse width | 475 | — |
| tW3 | REFRESH* pulse width | 675 | — |

All times given in nanoseconds.

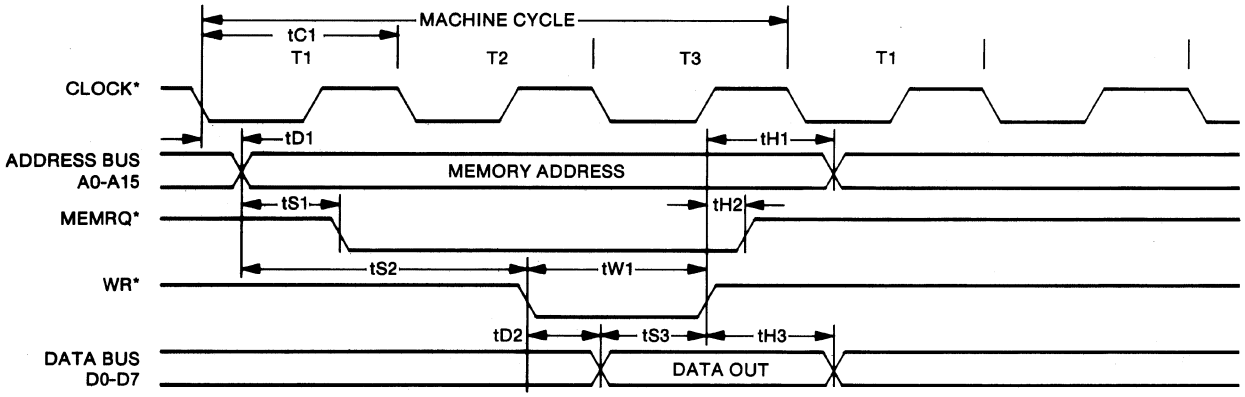
Figure 2-14. Opcode Fetch and Refresh Timing (78C13)




| SYMBOL | PARAMETER | MIN | MAX |
|---|---|---|---|
| tC1 | Clock cycle time | 400 | — |
| tD1 | Address delay from CLOCK* | — | 210 |
| tH1 | Address hold time after RD* inactive | 85 | — |
| tH2 | MEMRQ* hold time after RD* inactive | 0 | — |
| tH3 | Data hold time after RD* inactive | 0 | — |
| tS1 | Address setup before MEMRQ* active | 45 | — |
| tS2 | Address setup before RD* active | 105 | — |
| tS3 | Address setup before Data valid | 605 | — |
| tS4 | Data setup before RD* inactive | 320 | — |
| tW1 | RD* pulse width | 690 | — |

All times given in nanoseconds.

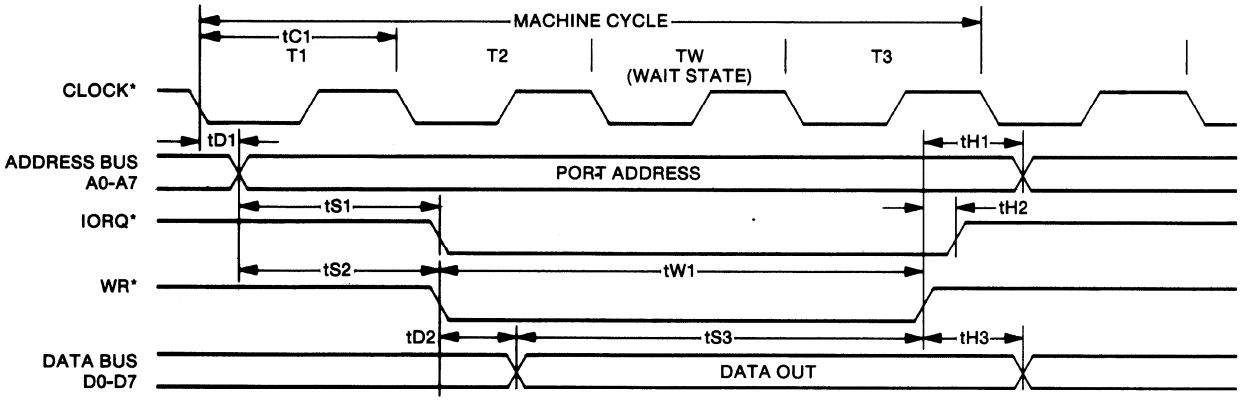
Figure 2-15. Memory Read Timing Other Than Opcode Fetch (78C13)




| SYMBOL | PARAMETER | MIN | MAX |
|---|---|---|---|
| tC1 | Clock cycle time | 400 | — |
| tD1 | Address delay from CLOCK* | — | 210 |
| tD2 | Data delay from WR* active | — | 140 |
| tH1 | Address hold time after WR* inactive | 85 | — |
| tH2 | MEMRQ* hold time after WR* inactive | 0 | — |
| tH3 | Data hold time after WR* inactive | 0 | — |
| tS1 | Address setup before MEMRQ* active | 45 | — |
| tS2 | Address setup before WR* active | 445 | — |
| tS3 | Data setup before WR* inactive | 265 | — |
| tW1 | WR* pulse width | 290 | — |

All times given in nanoseconds.

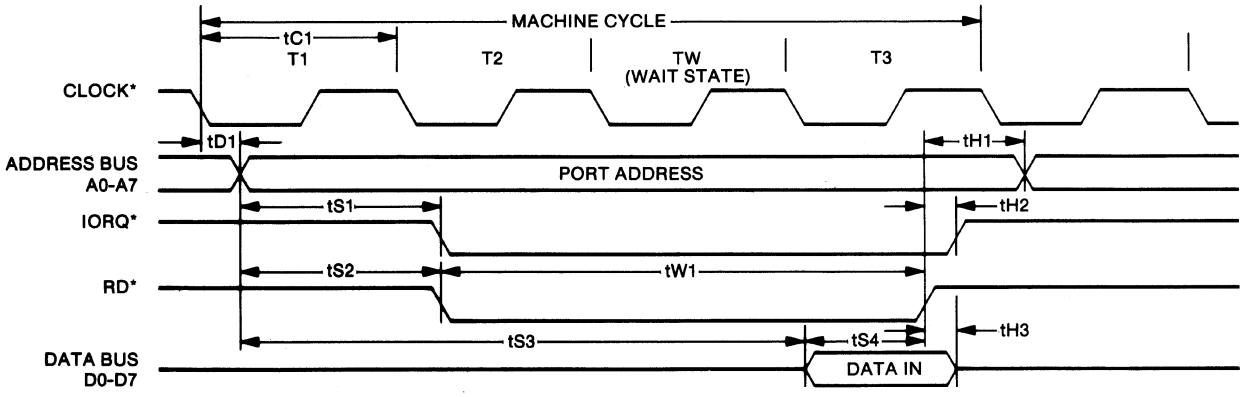
Figure 2-16. Memory Write Timing (78C13)




| SYMBOL | PARAMETER | MIN | MAX |
|---|---|---|---|
| tC1 | Clock cycle time | 400 | — |
| tD1 | Address delay from CLOCK* | — | 210 |
| tD2 | Data delay from WR* active | — | 140 |
| tH1 | Address hold time after WR* inactive | 85 | — |
| tH2 | IORQ* hold time after WR* inactive | 0 | — |
| tH3 | Data hold time after WR* inactive | 0 | — |
| tS1 | Address setup before IORQ* active | 245 | — |
| tS2 | Address setup before WR* active | 260 | — |
| tS3 | Data setup before WR* inactive | 880 | — |
| tW1 | WR* pulse width | 905 | — |

All times given in nanoseconds.

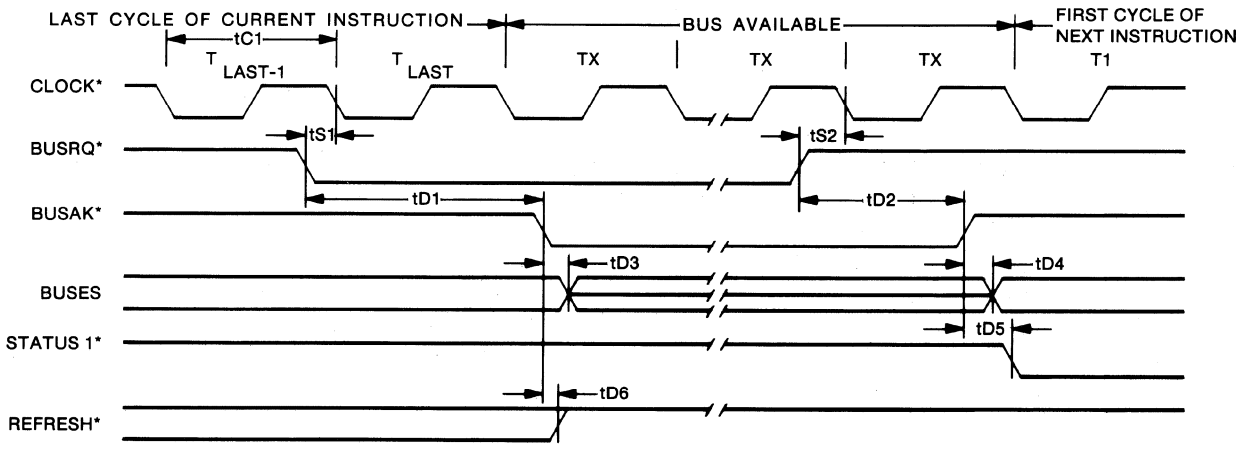
Figure 2-17. Output Timing (78C13)




| SYMBOL | PARAMETER | MIN | MAX |
|---|---|---|---|
| tC1 | Clock cycle time | 400 | — |
| tD1 | Address delay from CLOCK* | — | 210 |
| tH1 | Address hold time after RD* inactive | 85 | — |
| tH2 | IORQ* hold time after RD* inactive | 0 | — |
| tH3 | Data hold time after RD* inactive | 0 | — |
| tS1 | Address setup before IORQ* active | 245 | — |
| tS2 | Address setup before RD* active | 280 | — |
| tS3 | Address setup before Data valid | 1010 | — |
| tS4 | Data setup before RD* inactive | 320 | — |
| tW1 | RD* pulse width | 895 | — |

All times given in nanoseconds.

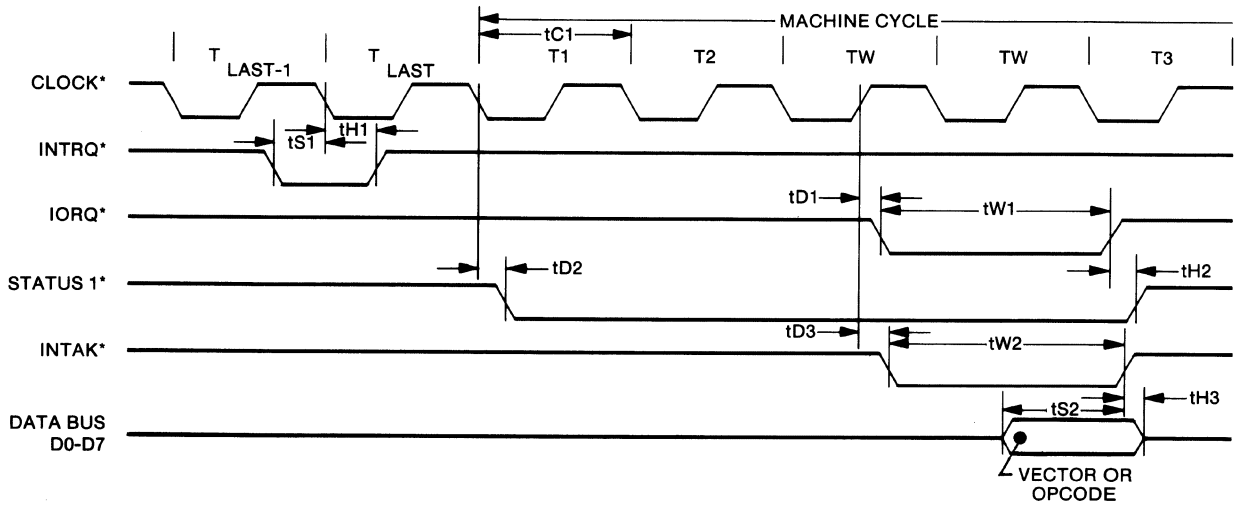
Figure 2-18. Input Timing (78C13)




| SYMBOL | PARAMETER | MIN | MAX |
|---|---|---|---|
| tC1 | Clock cycle time | 400 | — |
| tD1 | BUSAK* delay from BUSRQ* active | — | 800 |
| tD2 | BUSAK* inactive delay from BUSRQ* inactive | — | 595 |
| tD3 | Buses delay after BUSAK* active | — | 100 |
| tD4 | Buses delay after BUSAK* inactive | — | 340 |
| tD5 | STATUS 1* delay after BUSAK* inactive | — | 335 |
| tD6 | REFRESH* delay after BUSAK* active | — | 95 |
| tS1 | BUSRQ* active setup before last time state | 225 | — |
| tS2 | BUSRQ* inactive setup before last time state | 230 | — |

All times given in nanoseconds.

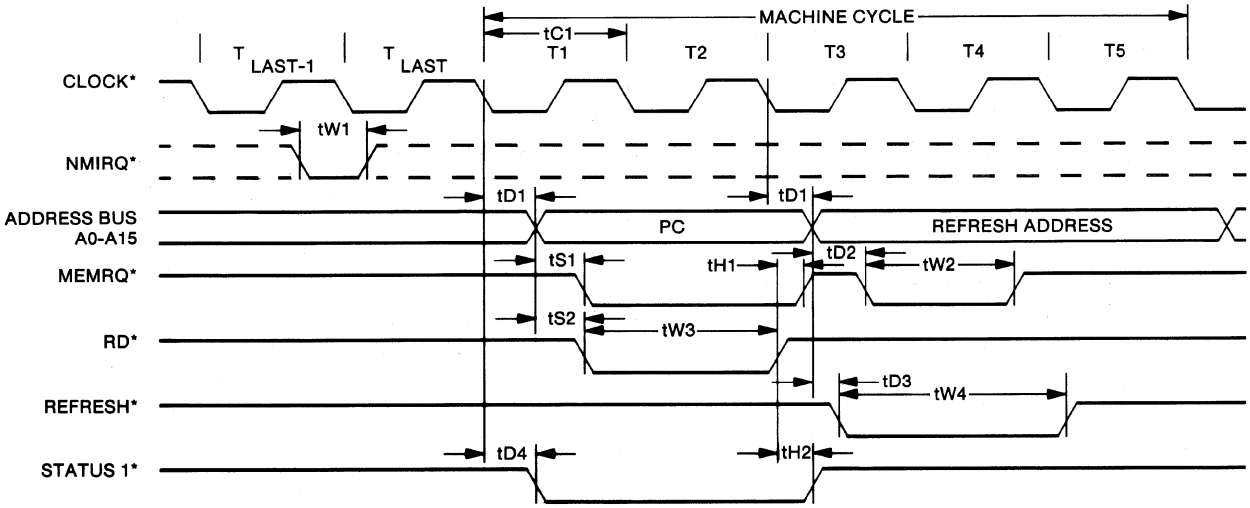
Figure 2-19. Bus Request Timing (78C13)




| SYMBOL | PARAMETER | MIN | MAX |
|---|---|---|---|
| tC1 | Clock cycle time | 400 | — |
| tD1 | IORQ* delay from CLOCK* | — | 165 |
| tD2 | STATUS 1* delay from CLOCK* | — | 195 |
| tD3 | INTAK* delay from CLOCK* | — | 190 |
| tH1 | INTRQ* hold time after last time state | 0 | — |
| tH2 | STATUS 1* hold time after IORQ* | 0 | — |
| tH3 | Data hold time after INTAK* inactive | 0 | — |
| tS1 | INTRQ* setup before last time state | 225 | — |
| tS2 | Data setup before INTAK* inactive | 330 | — |
| tW1 | IORQ* pulse width | 495 | — |
| tW2 | INTAK* pulse width | 480 | — |

All times given in nanoseconds.

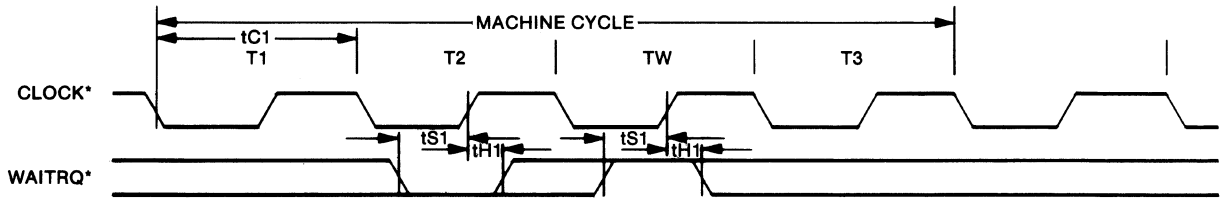
Figure 2-20. Interrupt Request Timing (78C13)




| SYMBOL | PARAMETER | MIN | MAX |
|---|---|---|---|
| tC1 | Clock cycle time | 400 | — |
| tD1 | Address delay from CLOCK* | — | 210 |
| tD2 | MEMRQ* delay from Refresh Address valid | — | 195 |
| tD3 | REFRESH* delay from Refresh Address valid | — | 100 |
| tD4 | STATUS 1* delay from CLOCK* | — | 195 |
| tH1 | MEMRQ* hold time after RD* inactive | 0 | — |
| tH2 | STATUS 1* hold time after RD* inactive | 0 | — |
| tS1 | Address setup before MEMRQ* active | 45 | — |
| tS2 | Address setup before RD* active | 105 | — |
| tW1 | NMIRQ* pulse width | 145 | — |
| tW2 | MEMRQ* pulse width (REFRESH) | 300 | — |
| tW3 | RD* pulse width | 475 | — |
| tW4 | REFRESH* pulse width | 675 | — |

All times given in nanoseconds.

Figure 2-21. Nonmaskable Interrupt Request Timing (78C13)




| SYMBOL | PARAMETER | MIN | MAX |
|---|---|---|---|
| tC1 | Clock cycle time | 400 | — |
| tH1 | WAITRQ* hold time after CLOCK* | 0 | — |
| tS1 | WAITRQ* setup before CLOCK* | 135 | — |

All times given in nanoseconds.

Figure 2-22. Wait State Timing (78C13)

## ELECTRICAL AND ENVIRONMENTAL SPECIFICATIONS

| PARAMETER | Recommended Operating Limits | | | Absolute Nonoperating Limits | | UNITS |
|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | MAX | |
| Supply voltage (Vcc) | 4.50 | 5.00 | 5.50 | 0 | 7.00 | Volts |
| Supply current (Icc)[1] | — | 75 | 190 | — | — | mA |
| Free air temperature | 0 | +25 | +70 | -40 | +100 | °C |
| Noncondensing relative humidity | 5 | — | 95 | 5 | 95 | %RH |

[1] Without onboard memory.

Figure 2-23. Electrical and Environmental Specifications (78C13)

| PIN NUMBER | | | | PIN NUMBER | | | |
|---|---|---|---|---|---|---|---|
| OUTPUT (CMOS LOADS DRIVEN) | | | | | OUTPUT (CMOS LOADS DRIVEN) | | |
| INPUT (CMOS LOADS) | | | | | | INPUT (CMOS LOADS) | |
| MNEMONIC | | | | | | | MNEMONIC |
| SEGMENT | | 20 | 2 | 1 | OUT | | GND |

Figure 2-24. Segment Connector Pin List (78C13)

| PIN NUMBER | | | | PIN NUMBER | | | |
|---|---|---|---|---|---|---|---|
| OUTPUT (CMOS LOADS DRIVEN) | | | | | OUTPUT (CMOS LOADS DRIVEN) | | |
| INPUT (CMOS LOADS)[1] | | | | | | INPUT (CMOS LOADS)[1] | |
| MNEMONIC | | | | | | | MNEMONIC |
| +5V | IN | | 2 | 1 | | IN | +5V |
| GROUND | IN | | 4 | 3 | | IN | GROUND |
| -5V | | | 6 | 5 | | | -5V |
| D7 | 1 | 20 | 8 | 7 | 20 | 1 | D3 |
| D6 | 1 | 20 | 10 | 9 | 20 | 1 | D2 |
| D5 | 1 | 20 | 12 | 11 | 20 | 1 | D1 |
| D4 | 1 | 20 | 14 | 13 | 20 | 1 | D0 |
| A15 | 1 | 20 | 16 | 15 | 20 | 1 | A7 |
| A14 | 1 | 20 | 18 | 17 | 20 | 1 | A6 |
| A13 | 1 | 20 | 20 | 19 | 20 | 1 | A5 |
| A12 | 1 | 20 | 22 | 21 | 20 | 1 | A4 |
| A11 | 1 | 20 | 24 | 23 | 20 | 1 | A3 |
| A10 | 1 | 20 | 26 | 25 | 20 | 1 | A2 |
| A9 | 1 | 20 | 28 | 27 | 20 | 1 | A1 |
| A8 | 1 | 20 | 30 | 29 | 20 | 1 | A0 |
| RD* | 1 | 20 | 32 | 31 | 20 | 1 | WR* |
| MEMRQ* | 1 | 20 | 34 | 33 | 20 | 1 | IORQ* |
| MEMEX | | 19 | 36 | 35 | OUT | | IOEXP |
| MCSYNC* | | 20 | 38 | 37 | 20 | | REFRESH* |
| STATUS 0* | | | 40 | 39 | 20 | | STATUS 1* |
| BUSRQ* | 2[2] | | 42 | 41 | 20 | | BUSAK* |
| INTRQ* | 2[2] | | 44 | 43 | 20 | | INTAK* |
| NMIRQ* | 2[2] | | 46 | 45 | | 2[2] | WAITRQ* |
| PBRESET* | 3 | | 48 | 47 | 20 | | SYSRESET* |
| CNTRL* | | | 50 | 49 | 20 | | CLOCK* |
| PCI | IN | | 52 | 51 | OUT | | PCO |
| AUX GND | | | 54 | 53 | | | AUX GND |
| AUX -V | | | 56 | 55 | | | AUX +V |

* Low-level active logic
[1] CMOS load = 10 pF at ±5 μA
[2] Load = 10 pF at 0.5 mA
[3] Switch input

Figure 2-25. STD Edge Connector (78C13)

# SECTION 3
# Operation and Programming

## INTRODUCTION

This section describes the theory of operation for the 78C13. The following describes the operation of the power-on/pushbutton reset circuit, and memory expansion (MEMEX and Segment) control. All references are made to the schematic in section 5.

## POWER-ON AND PUSHBUTTON RESET CIRCUIT

The 78C13 reset circuit consists mainly of two voltage comparators. The first comparator will not turn on until the power supply reaches a voltage in the operating range. After the first comparator turns on indicating a valid operating voltage, RESET* must be held low until the clock oscillator is functioning. This is accomplished by having the first comparator charge an RC network which forms an input to the second voltage comparator. The second comparator will turn on and set RESET* high after an RC time constant equal to the oscillator startup time (40 ms maximum).

R18 and U20 generate a reference voltage for the two comparators. R12 and R15 form a voltage divider for the supply voltage. R16 and C22 form the oscillator startup time RC time constant network. R7 and R13 provide hysteresis for the voltage comparators to prevent oscillations.

The remainder of the reset circuit is associated with a pushbutton reset. The pushbutton input is debounced, and then the reset pulse generated is limited to prevent any interference with refresh (pulse width = 30 $\mu$s typically).

PBRESET* is debounced by a circuit consisting of two comparators and an RC network. Both comparators are part of U17. It is debounced approximately 5 ms when the button is pressed and approximately 20 ms when it is released.

After it has been debounced, it triggers the first stage of U11 which is a one-shot. When this one-shot goes back to its normal state, it will trigger the second stage of U11. The first stage of U11 will return to its normal state either when it times out (approximately 400 ms) or when the M1* signal from the processor occurs. Normally the M1* signal will occur first and the reset pulse will be synchronized with it. If M1* does not occur, a reset signal will be generated anyway. When the second stage of U11 is triggered, it generates a pulse no more than 50 $\mu$s long which is ORed together with the Power-On Reset* signal and becomes RST*.

## MEMEX AND SEGMENT CONTROL

Both MEMEX and Segment allow the capacity of the system memory to be expanded. MEMEX is implemented through the STD BUS, whereas Segment is implemented through the user connector J1. Since MEMEX is on the STD BUS, it is a signal that can be used by any card. Segment, on the other hand, is only used when it is connected by cable to a card that responds to Segment. Other than this difference, MEMEX and Segment are the same. In the following theory description MEMEX is used, but the theory holds true for Segment as well.

MEMEX allows the user to select between two banks of memory. To use MEMEX, the program writes to the on-card port. MEMEX uses bit D0 of the port, and Segment uses bit D1. Writing to the port immediately affects the memory expansion line polarities. MEMEX affects the entire system, since it is an STD BUS signal. Segment affects only the card to which it is connected.

Figure 3-1 shows a system with 96K of memory. The on-card memory consists of four 8K x 8 ROMs residing at addresses 0000-7FFF. This memory is permanently enabled and can be addressed whether MEMEX is high or low. The other 64K block is RAM and is divided into two 32K banks on separate cards. Both banks reside at addresses 8000-FFFF. One bank is enabled by MEMEX low and the other is enabled by MEMEX high. With this scheme, the main part of the software driver can reside in the on-card memory at addresses 0000-7FFF. This main program will use MEMEX to switch back and forth between the two banks of RAM.

Figure 3-2 shows a system with 128K of memory split into two 64K banks. Both banks reside at addresses 0000-FFFF. The on-card memory sockets of the 78C13 are not used, and are disabled by removing the associated jumpers (see section 2, **Installation and Specifications**). Therefore, MEMEX does not affect the on-card memory at all. The software drivers for this system must be located in both banks of memory, because once control is switched to the other bank there is no way to get back without the driver. For example, if the system driver program in the primary bank changed MEMEX high and there was no driver in the secondary bank, there would be no instructions to send MEMEX low and send the processor back to the primary bank. There must be some kind of memory bank control in both banks.

When switching MEMEX, the address of the present memory location does not change. For example, in the system shown in figure 3-2, if the program counter that holds the address of the next instruction were pointing at 4000 in the primary memory bank and MEMEX were switched high, the program counter would still be pointing to 4000, but in the secondary memory bank. Once at that point, any instruction may be executed, but it must be located at address 4000. To use MEMEX you must know where you are in memory in both banks so control is not lost switching between banks.

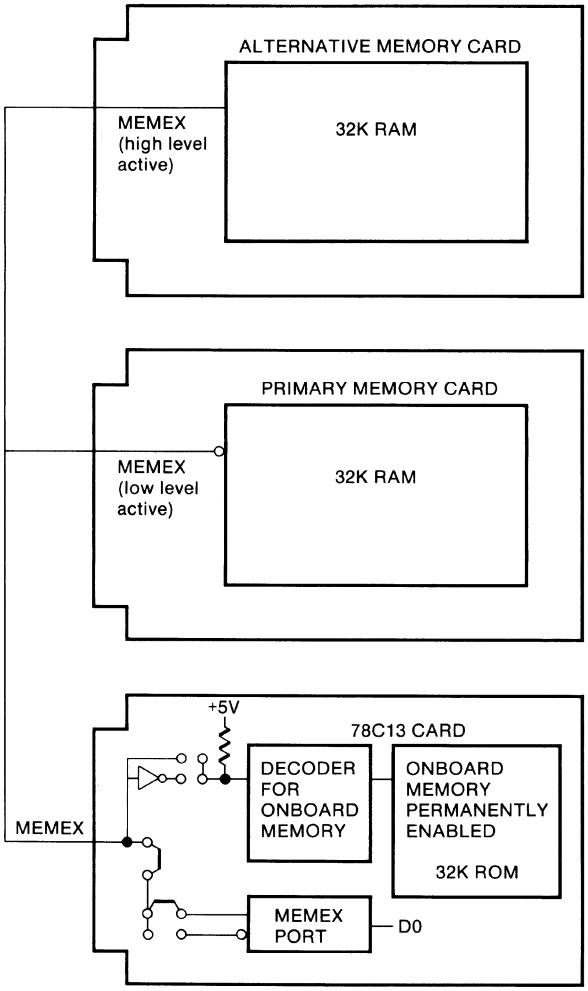



Figure 3-1. Example of MEMEX for Selecting Between Two Banks of Memory in a 96K Memory System

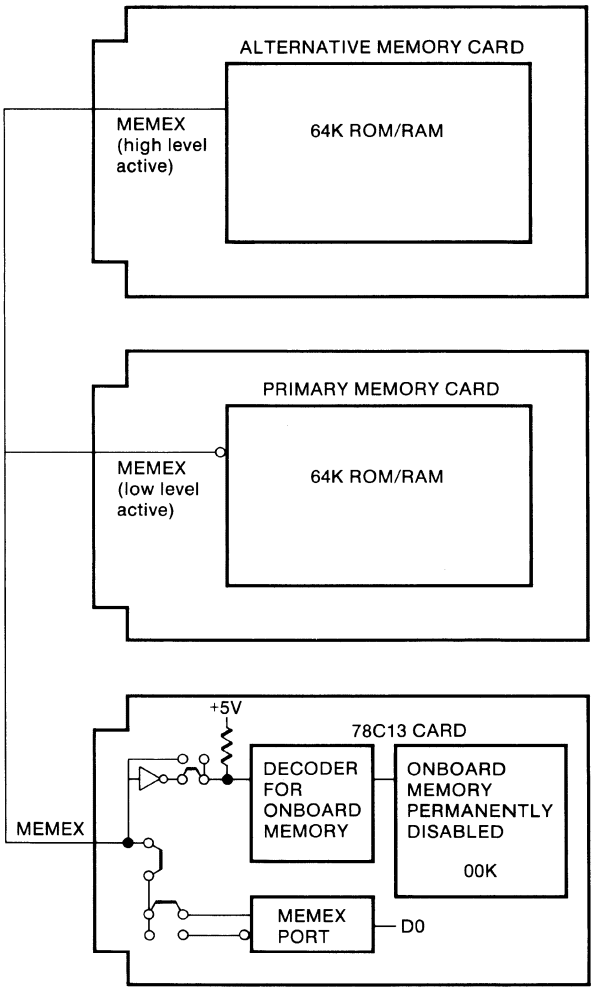



Figure 3-2. Example of MEMEX for Selecting Between Two Banks of Memory in a 128K Memory System

# SECTION 5
# Maintenance

## REFERENCE DRAWINGS

The schematic (figures 5-1 and 5-2) and assembly drawing (figure 5-3) in the following pages are included in this manual FOR QUICK REFERENCE ONLY. Because improvements may have been made after this manual was published, they may differ in some respects from the card and documentation that the user received from Pro-Log.

The schematic and the assembly drawing shipped by Pro-Log with the card are those from which the card was manufactured.

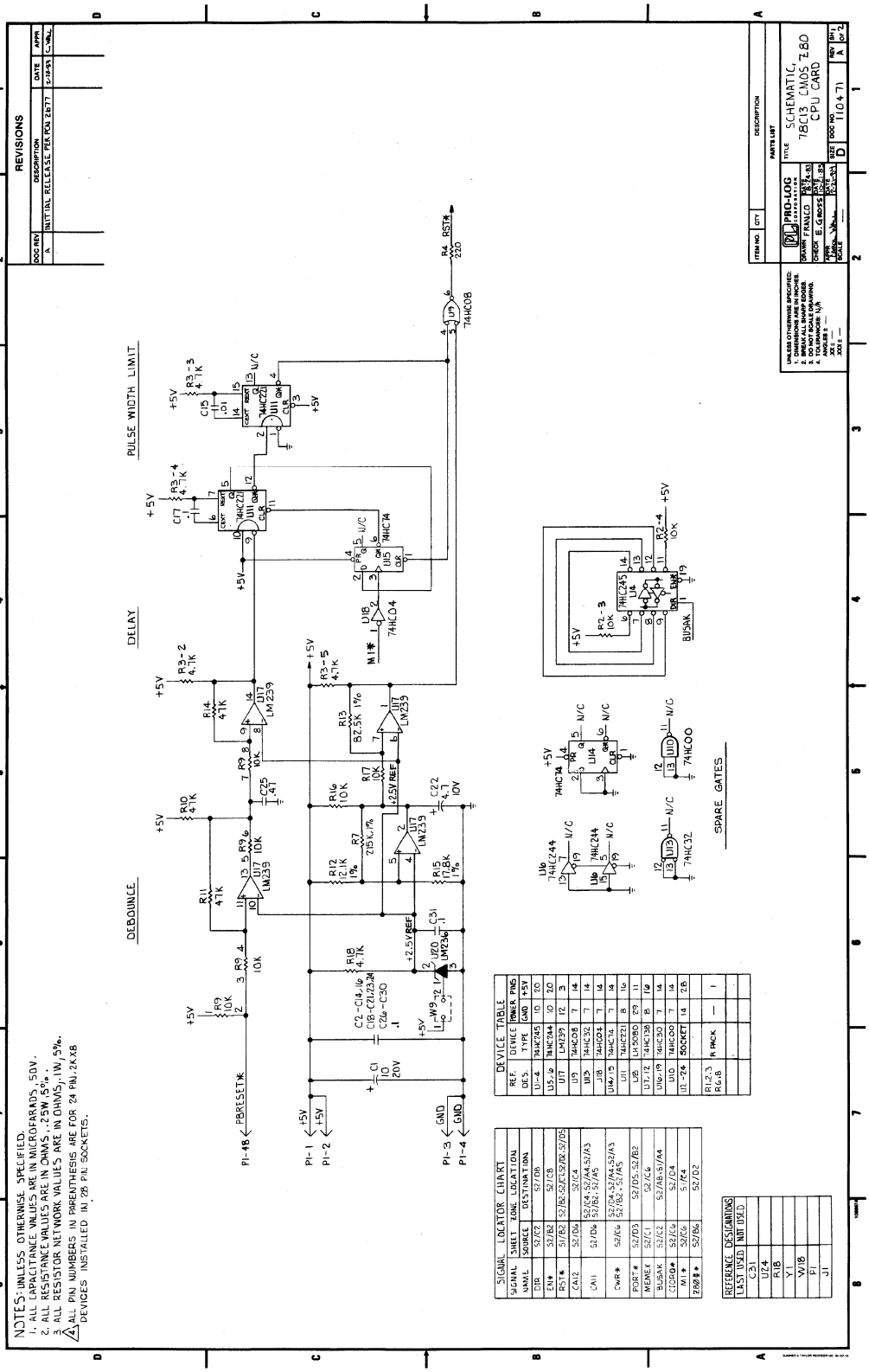
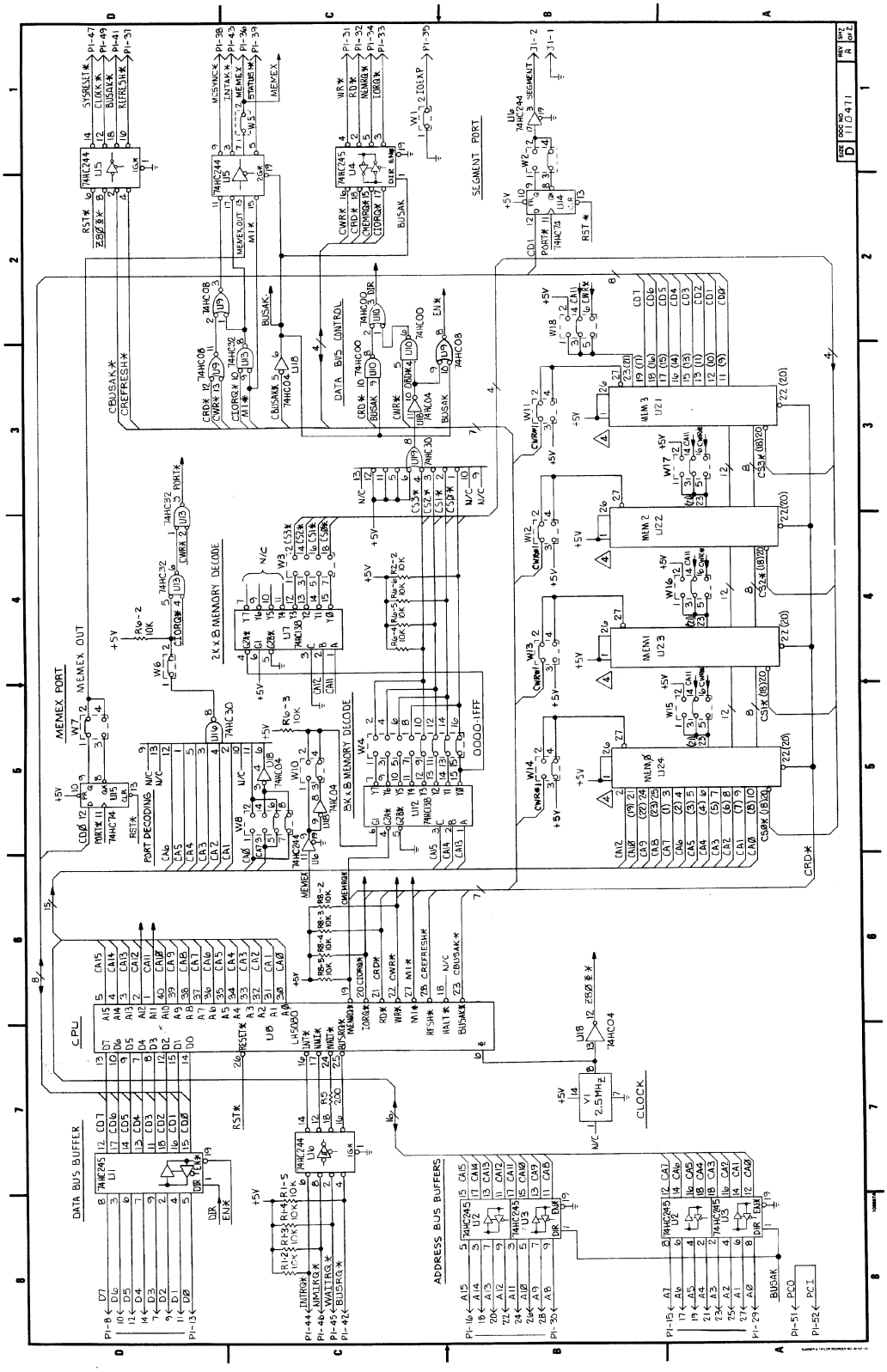
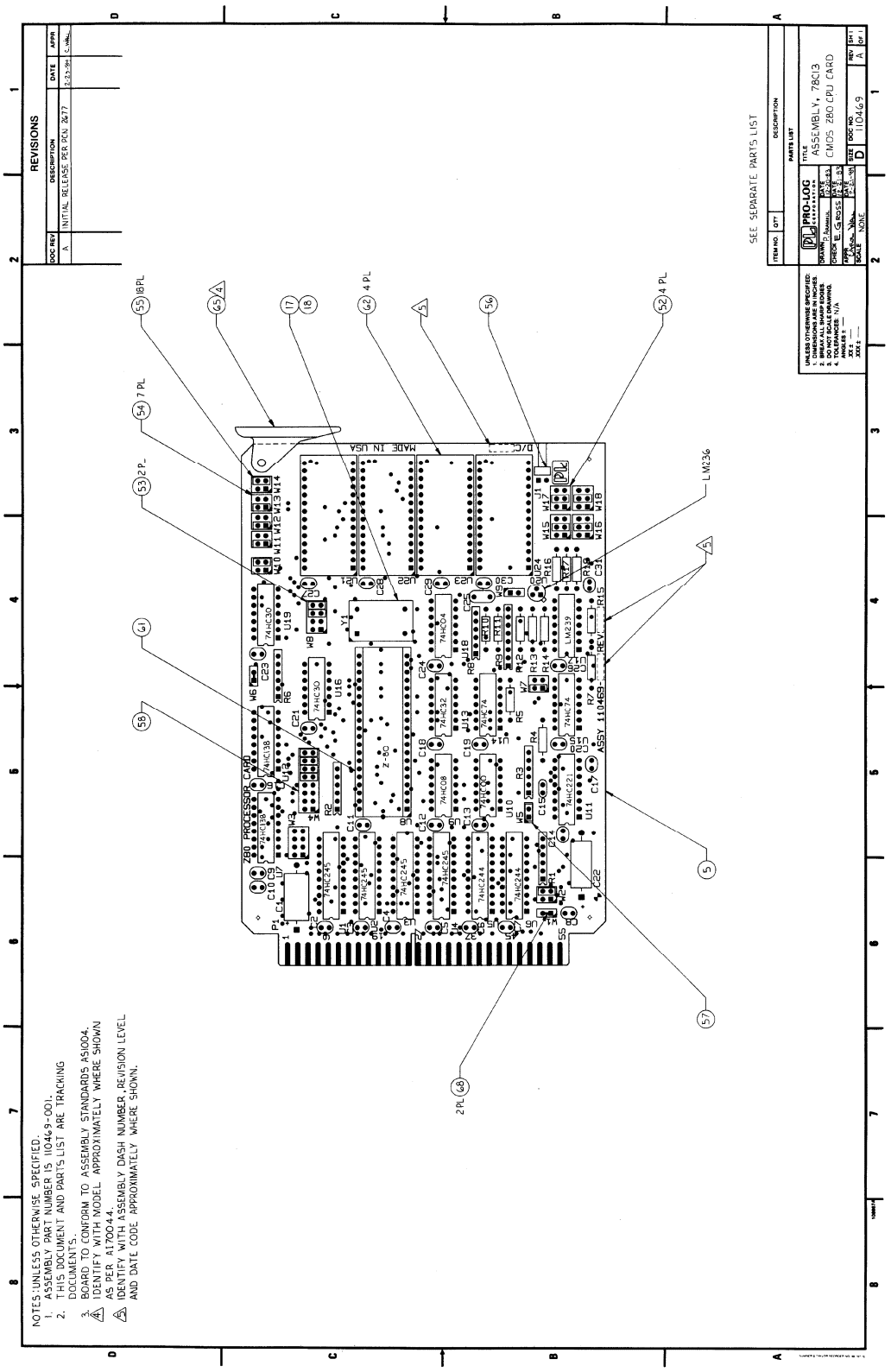

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 50V.
2. ALL RESISTANCE VALUES ARE IN OHMS, .25W, 5%.
3. ALL RESISTOR NETWORK VALUES ARE IN OHMS, 1W, 5%.
4. ALL PIN NUMBERS IN PARENTHESIS ARE FOR 24 PIN, 2K XB DEVICES INSTALLED IN 28 PIN SOCKETS.
REVISIONS
DESCRIPTION
INITIAL RELEASE PER POU 2677
PRO-LOG
SCHEMATIC, 78C13 CMOS Z80 CPU CARD
DEBOUNCE
DELAY
PULSE WIDTH LIMIT
SPARE GATES
SIGNAL LOCATOR CHART
DEVICE TABLE
REFERENCE DESIGNATIONS
(FOR REFERENCE ONLY)

Figure 5-1. Schematic Sheet 1 (78C13)



(FOR REFERENCE ONLY)

**Figure 5-2. Schematic Sheet 2 (78C13)**




(FOR REFERENCE ONLY)

**Figure 5-3. Assembly Drawing (78C13)**

## RETURN FOR REPAIR PROCEDURES

### Domestic Customers:

1. Call Customer Support at (800) 538-9570, ext. 3617. In California call (408) 646-3617 from 7 a.m. to 3 p.m. (PST).
2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment (if applicable), reason for return, and the name and telephone number of the person we should contact (preferably the user), if there are further questions.
4. Pack the equipment in a solid cardboard box secured with packing material.

**CAUTION**

Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during shipment. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, California 93940

   Reference CRO #_____

### International Customers:

Equipment repair is handled by your local Pro-Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

## Limited Warranty

**Limited Warranty:** Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. The liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned f.o.b. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller or the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

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